L Number	Hits	Search Text	DB	Time stamp
1	2	(("5638334") or ("5359570")).PN.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 17:59
2	8883	((365/185.09) or (365/200) or (365/225.5) or (365/230.03) or (365/231) or (365/238.5) or (365/243.5) or (711/203) or (711/205) or (711/206) or (711/207) or (711/208) or (711/209) or (711/213) or (711/217) or (711/221) or (714/8) or (714/710) or (714/752)).CCLS.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:00
3	207	(((365/185.09) or (365/200) or (365/225.5) or (365/230.03) or (365/231) or (365/238.5) or (365/243.5) or (711/203) or (711/205) or (711/206) or (711/207) or (711/208) or (711/209) or (711/213) or (711/217) or (711/221) or (714/8) or (714/710) or (714/752)).CCLS.) and ((address adj conversion) or (address adj translation)) and (range adj3 address)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:02
4	182	(((365/185.09) or (365/200) or (365/225.5) or (365/230.03) or (365/231) or (365/238.5) or (365/243.5) or (711/203) or (711/205) or (711/206) or (711/207) or (711/208) or (711/209) or (711/213) or (711/217) or (711/221) or (714/8) or (714/710) or (714/752)).CCLS.) and ((address adj conversion) or (address adj translation)) and (range adj2 address)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:03
5	43	(((365/185.09) or (365/200) or (365/225.5) or (365/230.03) or (365/231) or (365/238.5) or (365/243.5) or (711/203) or (711/205) or (711/206) or (711/207) or (711/208) or (711/209) or (711/213) or (711/217) or (711/221) or (714/8) or (714/710) or (714/752)).CCLS.) and ((address adj conversion) or (address adj translation)) and (range adj2 address) and (block adj address)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:04
6	5	(((365/185.09) or (365/200) or (365/225.5) or (365/230.03) or (365/231) or (365/238.5) or (365/243.5) or (711/203) or (711/205) or (711/206) or (711/207) or (711/208) or (711/209) or (711/213) or (711/217) or (711/221) or (714/8) or (714/710) or (714/752)).CCLS.) and ((address adj conversion) or (address adj translation)) and (range adj2 address) and (block adj address) and (row adj address) and (segment adj address)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:09
7	1030	MRAM	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:22
9	5	(((365/185.09) or (365/200) or (365/225.5) or (365/230.03) or (365/231) or (365/238.5) or (365/243.5) or (711/203) or (711/205) or (711/206) or (711/207) or (711/208) or (711/209) or (711/213) or (711/217) or (711/221) or (714/8) or (714/710) or (714/752)).CCLS.) and MRAM and (address adj (conversion or translation))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:10
8	56	(((365/185.09) or (365/200) or (365/225.5) or (365/230.03) or (365/231) or (365/238.5) or (365/243.5) or (711/203) or (711/205) or (711/206) or (711/207) or (711/208) or (711/209) or (711/213) or (711/217) or (711/221) or (714/8) or (714/710) or (714/752)).CCLS.) and MRAM	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:12

10	358	MRAM and address	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:23
11	11	MRAM and (address adj range)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:28
12	54	((block adj address) adj data) and ((logical or virtual or effective) adj address) and (physical adj address)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/15 18:30

DOCUMENT-IDENTIFIER: US 20010017798 A1

TITLE: Semiconductor integrated circuit device and data processor device

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365/200

[0034] We shall describe a memory device or data processor device of the first embodiment according to the invention. FIGS. 2 are conceptual diagrams of a memory array portion of the memory device. As shown in FIG. 2a, a peripheral circuit 51 such as a sense amplifier and driver is built on a silicon substrate surface, and a memory cell array 52 is provided thereon with an insulator film interposed therebetween. According to this construction, a small-area memory device can be produced as compared with the case where the memory cell array and the peripheral circuit are formed on the same plane. Also, this construction is suited for fast operation because the memory cell array and the peripheral circuit can be connected by short conducting lines. The memory cell array on the insulator film is not limited to semiconductor memories, but may be memories made of other materials such as MRAM (magnetic random access memory). The MRAM stores information by utilizing a phenomenon that the resistance of a conductor which consists of stacked two magnetic films changes or a tunnel current between the magnetic films changes, when the magnetization directions of the magnetic films are parallel or anti-parallel.

DOCUMENT-IDENTIFIER: US 20010014039 A1

TITLE: MEMORY TILE FOR USE IN A TILED MEMORY

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365/200

[0043] FIG. 4 illustrates in block diagram form memory tile 22 of FIG. 1, which is in accordance with one embodiment of the present invention. In this particular embodiment, memory tile 22 includes address decode circuitry 32a, 32b, 32c', 32c", sense amplifier circuitry 34, data input/output circuitry 36, redundancy circuitry 38a and 38b, charge source circuitry 24a, voltage level detector 24b, access control logic circuitry 42a, 42b, and memory cells 44. Memory cells 44 maybe dynamic random access memory (DRAM) cells, static random access memory (SRAM) cells, ferroelectric random access memory (FeRAM) cells, magnetoresistive random access memory (MRAM) cells, or electrically erasable read only memory (EEPROM) cells, read only memory (ROM) cells, or other memory cells which are arranged in an array of rows and columns, and randomly accessible.